COMPARISON OF THE INTERFACIAL THERMAL RESISTIVITY OF SILVER AND SOLDER DIE-ATTACH USING LASER FLASH TECHNIQUE

Zhiye (Zach) Zhang, Jesus Noel Calata, Carlos Suchicital, Guo-Quan Lu and D.P.H. Hasselman
The Bradley Department of Electrical and Computer Engineering and
Department of Materials Science and Engineering
Virginia Polytechnic Institute and State University
Whittemore Hall 658
Blacksburg, VA 24061 USA
Phone: (540) 231-8423
Fax: (540) 231-6579
Email: zachzhang@vt.edu

ABSTRACT

Silver as a die-attach material is a promising alternative to solder as demonstrated by pressure-assisted sintering experiments on silver paste. Unlike solder, the higher operating temperature capability of silver makes it suitable for high-temperature power-device applications. The laser flash technique, which is widely used to determine thermal diffusivity of materials, was used to obtain the interfacial thermal resistances from the silver and solder-attached materials. The measurements were obtained from samples consisting of the die-attach material sandwiched between copper discs. By measuring the half-temperature rise-time of the sample's backside following the incidence of the laser-flash on the front, the thermal resistance contribution arising from the presence of the die-attach layer was obtained by analytical method. Finite element modeling (FEM) as a numerical method provided the identical results with the analytical method. It was found that using silver as the die-attach layer can almost eliminate the interfacial thermal resistance of the die-attach layer. Coating the copper substrate with gold also reduced the interfacial thermal resistance to about one-third when using reflowed solder as die-attach layer.

KEY WORDS: interfacial thermal resistance, laser flash technique, silver die-attach, solder die-attach

NOMENCLATURE

a thermal diffusivity, cm^2/s
c specific heat, J/g-°C
d or D thickness, cm
h heat transfer coefficient, $W/(K*cm^2)$
κ thermal conductivity, W/(cm-K)
T temperature, K
Ri interfacial thermal resistivity, $(K*cm^2/W)$

Greek symbols

ρ mass density (g/cm^3)

INTRODUCTION

New applications in power electronics and other electronic systems require increasingly higher level of power. At the same time, packages and devices are progressively becoming smaller such that more efficient heat transport is required to cope with the increased power density. Power semiconductor devices - the major heat sources - are usually attached to the substrate with a solder layer that is several mils thick. The die-attach layer also serves as an electrical interconnection and the primary heat transport path. The most common solder composition comes from the Pb-Sn binary system and more recently from lead-free systems such as tin-silver. Compared with other metals used in electronic substrates and packages such copper, gold and silver, solder alloys have relatively poor thermal conductivities. Interconnections formed with solder also have high interfacial thermal resistance. The high interfacial thermal resistance may be caused by large voids at the interface, poor bonding due to the mismatched crystal structure, poor wetting of the substrate by the solder due to oxidation and contamination, and possibly a large difference in Young's modules across the interface that prevents heat transport carried by phonons.

Metal pastes such as silver, gold, or copper, are commonly used in the fabrication of hybrid and cofired microelectronic packages. These metals have high electrical and thermal conductivities. Sintering metal paste can, in principle, appreciably reduce the interfacial thermal resistance because sintering, an atomic diffusion process, can produce the voids-free joint and good chemical bonding. Since there is no liquid phase involved, wetting is less of an issue during sintering. Copper, silver and gold have the same crystal structure and very close lattice parameters and Young's modules, such that heat carried by both electrons and phonons can dissipate more easily through the interfaces. However, these metals normally must be processed or sintered at high temperatures (>600°C) to be useful as conductors. Several studies [1-8] have been made to evaluate the use of pressure to lower the sintering temperature of silver paste in order to serve as the attachment layer for power semiconductor devices. The results have been encouraging and the absence of large voids could mean

substantial reduction in interfacial thermal resistance. This study aims to show that pressure-assisted low-temperature sintering of silver paste can virtually eliminate the interfacial thermal resistance. The laser flash technique, which is widely used to determine thermal diffusivity of materials, was applied to obtain the interfacial thermal resistance for the silver and solder-attached materials using similarly prepared specimens consisting of the die-attach material sandwiched between copper discs.

FLASH TECHNIQUE

The laser flash technique schematically shown in Fig. 1 is based on the measurement of the thermal transient of the specimen's backside surface when a pulsed laser illuminates the front. With this arrangement, it is possible to avoid interferences between the thermal sensor and the heat source [9]. If the specimen is a homogenous material without interfacial thermal resistance, the thermal diffusivity can be obtained from the well-known Parker equation [10]:

$$a = \left(0.139 * d^2\right) / t_{1/2} \tag{1}$$

where a is the thermal diffusivity, d is the thickness of the sample and $t_{1/2}$ is the half-temperature rise-time of the specimen's backside.

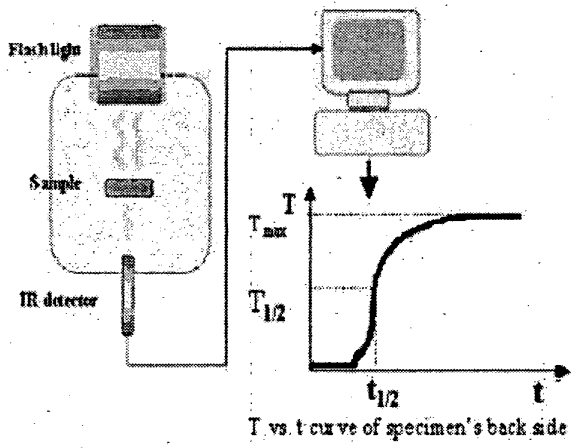

Fig. 1. Schematic for measuring thermal diffusivity by the laser flash technique.

Applying this method to measure the interfacial thermal resistance, shown in Fig. 2, is more complex. Firstly, we assume the laser flash is an ideal heat pulse with homogenous heat distribution in the Y-Z plane and heat flows from the front to back surface of the specimen. The thickness of die-attach layer, compared with top copper layer 1 and bottom copper layer, is too thin and thus the thermal capacity of the die-attach layer is negligible. The differential equations for heat diffusion that must be solved are given in Equations 2 and 3; Equations 4,5 and 6 are the boundary conditions, Equation 7 is the initial condition, equations 8 and 9 are the well-known relations between thermal conductivity and thermal diffusivity in each homogeneous material 1 and 2.

$$a\frac{\partial^2 T_1(x,t)}{\partial x} = \partial\frac{T_1(x,t)}{\partial t} \tag{2}$$

$$a\frac{\partial^2 T_2(x,t)}{\partial x} = \partial\frac{T_2(x,t)}{\partial t} \tag{3}$$

$$-k\frac{\partial T_1(-d_1,t)}{\partial x} = q(t) \tag{4}$$

$$-k\frac{\partial T_1(0,t)}{\partial x} = -k\frac{\partial T_2(0,t)}{\partial x} = h(T_1(0,t) - T_2(0,t)) \tag{5}$$

$$-k\frac{\partial T_1(d_2,t)}{\partial x} = 0 \tag{6}$$

$$T_1(x,0) = T_2(x,0) = 0 \tag{7}$$

$$k_1 = a_1 * \rho_1 * c_1 \tag{8}$$

$$k_2 = a_2 * \rho_2 * c_2 \tag{9}$$

where T is the temperature, t is the time, κ is the thermal conductivity and q is the flash energy illuminating onto the unit specimen, h is the heat transfer coefficient, and thus $1/h$ is the thermal resistance per area caused by die-attach layer, a is thermal diffusivity, ρ is the density and c is specific heat. The heat transfer coefficient h can be expressed as a function of a_1, ρ_1, c_1, d_1, a_2, ρ_2, c_2, d_2 and $t_{1/2}$, by solving the above differential equations. Obviously, the thermal resistance per area caused by die-attach layer, $1/h$ can be calculated once we measure $t_{1/2}$ and know the materials' properties. Several $1/h$ with different thickness of the die-attach layer can be obtained and the intercept at zero thickness (R_i) represents the interfacial thermal resistivity of the die-attach layer. Hung Joo Lee [11] gave the solution of the heat transfer equation and numerical-analysis software was developed to calculate the heat transfer coefficient.

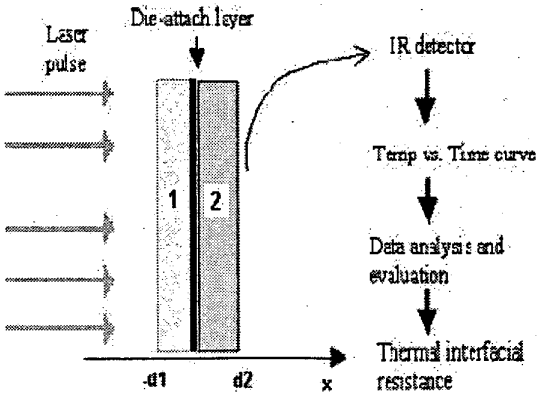

Fig. 2. Schematic for measuring interfacial thermal resistance in a bilayer structure with a thin attachment layer.

Electronic packages and modules have more complex structures than the bilayer samples commonly tested by the flash method such that applying the current analytical method to these structures is correspondingly much more difficult and complicated. On the other hand, finite element methods are employed in tasks where analytical solutions are difficult to obtain or are non-existent. Modeling software, such as I-DEAS™ and ANSYS™ are widely used to simulate and solve thermal problems and we are developing a FEM technique that will allow the application of the flash method to more complicated structures and while obtaining more accurate results [12].

The main experimental uncertainty of the laser flash technique to measure homogeneous materials is the effects of the finite laser pulse width and/or heat losses by radiation. Correction procedures for these effects were developed accordingly. Watt [13] offered several analytical solutions for 1D and 2D heat transfer through the sample, considering at the same time the different effects. Gembarovic and Taylor [14] utilized Laplace transformation for data reduction in the flash method. Beedham *et al.* [15] and McKay *et al.* [16] investigated errors originating from the non-uniformity of the laser pulse energy, while Hasselman and Donaldson [17] studied the effects of detector nonlinearity and sample sizes using a graphite thermal conductivity standard. With the applied correction procedure, the error can be controlled within 5%.

EXPERIMENTAL PROCEDURE

The samples for laser flash measurements were prepared by bonding copper discs with either Pb-Sn solder or silver. To fabricate the silver connected discs, the silver paste was sintered under an applied pressure using a set-up similar to that shown in Fig. 3 which was used by Zhang and Lu [6-8] to investigate pressure assisted sintering of silver paste at low temperature. To ensure good bonding, the copper discs were plated with a thin layer of gold using an electroless gold bath since the silver paste does not contain flux and is unable to clean the copper surface. The sintering process was carried out in air at 240°C under a 40 MPa external pressure for 5 minutes and allowed to cool in air. The solder-attached samples were fabricated by reflowing the sandwiched solder paste in a belt-type Sikama reflow oven following the typical heating profile for eutectic Pb-Sn solder reflow with a peak temperature of 210°C. The copper discs in one set of samples were soldered bare while the discs in another set were plated with gold using the same procedure used for the discs in the sintered silver-attached samples. Gold coating by Electroless plating results in the relatively good bonding and the thickness of coated gold is only about half micron, and thus the thermal effect of the coated gold to the whole specimen is negligible. The thickness of the solder layer was controlled by varying the amount of solder paste and by embedding several high-lead solder balls in the paste layer. Excess solder on the edges were polished off and the samples were cleaned with an aqueous flux cleaner.

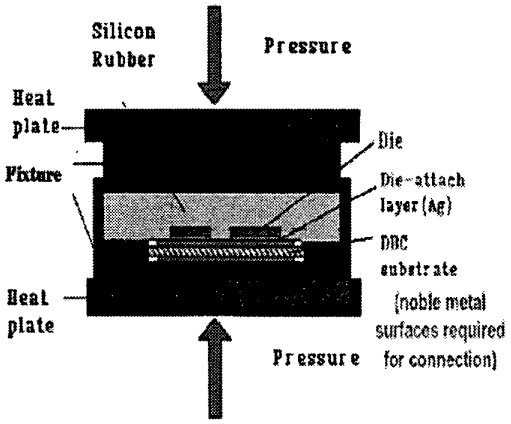

Fig. 3. Schematic of a fixture used for sintering under quasi-hydrostatic conditions.

The discs were then bonded using reflowed solder (Pb-Sn) or sintered silver to form the samples for interfacial thermal resistance measurement. The resulting structure is shown in Fig. 4 and except for the absence of a silicon device, is structurally similar to device die-attach structures. The diameter of the shown sample is 25.4 mm. Three types of samples were fabricated: solder-attached bare copper discs, solder-attached gold-plated copper discs, and sintered silver-attached gold-coated copper discs. The thickness of each sample was measured with a digital micrometer. The thickness of the solder layer was obtained by subtracting the thickness of the copper discs. The calculated solder thickness had an estimated error of ± 2 μm. Half-temperature rise-times of the samples were measured using the laser flash apparatus, and the heat transfer coefficient contribution from the attachment layers were calculated using the analytical software available with the experimental apparatus. Finally, the interfacial thermal resistance was obtained from the calculated thermal resistance by extrapolating the linear fit to zero thickness.

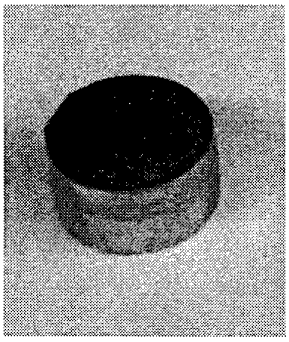

Fig. 4. Copper-solder-copper sample used in the laser flash experiments for obtaining the interfacial thermal resistance.

RESULTS AND DISCUSSION

Fig. 5 shows the thermal resistance per unit area (1/h) caused by the die-attach layer. The results obtained from the soldered discs show an increasing trend in the thermal resistance with increasing die-attach thickness. This indicates that the thermal resistance is an additive value of the interfacial resistance and the thermal resistance of the solder die-attach material. The results from both gold-plated and non-plated discs show a linear trend. Linear extrapolation of the data to zero thickness will yield the interfacial thermal resistivity. The gold-plated interface showed an improvement in the interfacial resistivity, which though small compared to the layer resistance, is nearly one-third that of the non-plated disc interface. At a 200 μm solder-attach layer thickness, the interfacial thermal resistance accounts for one-third of the total thermal resistance when the discs are gold-coated as compared to 42% when the discs are not coated. The improvement is most likely the result of better wetting of the surface by the solder resulting in good contact and lesser incidence of large voids, a common occurrence in sandwiched reflowed solder. The latter number is of comparable magnitude to results obtained by Haque [18] on solder-attached heat sink-to-package structure, where the temperature profile through the structure was monitored using thermocouples inserted at various locations.

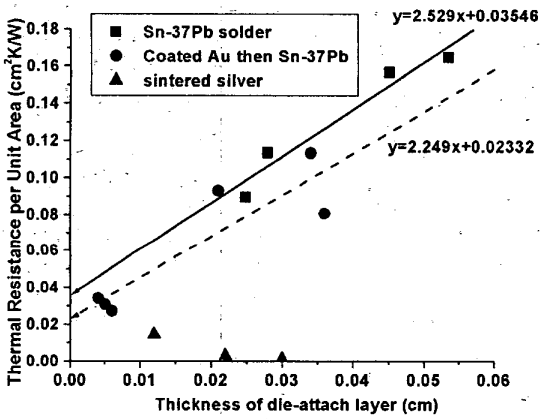

Fig. 5. Plots of the thermal resistance per unit area versus thickness of the die-attach layer.

The third set of data points were obtained from the sintered-silver attached discs. The thermal resistivity of silver (and hence sintered silver) is very small compared to that of solder such that the contribution of the silver layer to the total thermal resistance is likewise very small over the layer thickness range that was measured. The measured total thermal resistance is very small such that any change with thickness fell within the error of the instrument. For practical purposes, it can be assumed that the measurements represent the interfacial thermal resistivity of the silver-attached discs. This number is still lower than the best result from the solder-attached discs, that of the gold-plated discs. The lower thermal resistivity may be attributed to the extensive formation of a chemically bonded interface between the silver and gold and the absence of large voids that can hinder heat flow [7-8].

It is possible to obtain the uncertainty/error bar for the thermal resistance of monolithic materials with reasonable accuracy, but it is difficult to do so with composite structures. While it is possible to obtain reasonable numbers for the input parameters, how the analysis software magnifies the uncertainties is difficult to predict because of the non-linearities in the equations used.

CONCLUSION

The experimental work demonstrated that the laser flash technique can be used to determine the attachment layer material thermal resistance in a sandwiched structure similar to that of packaged semiconductor devices. Additionally, the technique made it possible to determine by extrapolation the contribution of the interface to the thermal resistance. Comparative measurements of thermal resistance on reflowed solder and sintered-silver attached copper discs showed that sintered silver not only had an overall lower thermal resistance but also a lower interfacial resistivity over that of solder. The lower interfacial resistivity may be attributed to better bonding of the interface through the formation of chemical bonds and the absence of large voids extending to the interface. The results also demonstrated that coating the copper substrate with gold reduced the interfacial resistivity by one-third. The improvement is due to enhanced wetting of the surface because of the ability of the gold to withstand oxidation at the reflow temperature of the solder, and hence a reduction in the likelihood of void formation.

Acknowledgement

The authors would like to thank John Bai for his work on the FEM simulation/verification and helpful discussions. This work was supported primarily by the ERC Program of the National Science Foundation under Award Number EEC-9731677.

References:

[1] H. Schwarzbauer "Novel Large Area Joining Technique for Improved Power Device Performance," *IEEE Transactions on Industrial Applications*, Vol. 27, No. 1, (1991), pp. 93-95.

[2] H. Schwarzhauer, "Method of Securing Electronic Components to a Substrate," *US Patent No. 4810672.*

[3] R. Kuhnert, and H. Schwarzbauer, "A Novel Packaging Technology for Large Area IC-Power Devices," *So. Cal-ISHM Symposium*, Anaheim, CA, April 1989.

[4] S. Klaka, and R. Sitting, "Reduction of Thermo-Mechanical Stress by Applying a Low Temperature Joining Technique," *Proceedings of the 6th International Symposium on Power Semiconductor Devices and ICs*, March 1994, pp. 259-264.

[5] U. Scheuermann, et al., "Low Temperature Joining Technology - A High Reliability Alternative to Solder Contacts," *Workshop on Metal Ceramic Composites for Functional Application, Vienna 4/5*, June 1997.

[6] Z. Zhang, and G-Q. Lu, "Pressure-Assisted Low-Temperature Sintering of Silver paste as an Alternative Die-Attach Solution to Solder Reflow," *Proceedings of the 2002 CPES Power Electronics Seminar, Blacksburg, VA.*

[7] Z. Zhang, and G-Q. Lu, "Pressure-Assisted Low-Temperature Sintering of Silver Paste as an Alternative Die-Attach Solution to Reflow," *The Fifth International IEEE Symposium on High Density Packaging and Component Failure Analysis in Electronics Manufacturing (HDP 2002).*

[8] Z. Zhang, and G-Q. Lu, "Pressure-Assisted Low-Temperature Sintering of Silver Paste as an Alternative Die-Attach Solution to Solder Reflow," *IEEE Transactions on Electronics Packaging Manufacturing* 25 (4) 279-283, October 2002.

[9] J. A. Cape and G. W. Lehman, "Temperature and finite pulse-time effects in the flash method for measuring thermal diffusivity," *J. Appl. Phys.*, 34 (1963), pp1909-1913.

[10] W.J. Parker, R.J. Jenkins, C.P. Butler, G.L. Abbott, "Flash Method of Determing Thermal Diffusivity, Heat Capacity and Thermal Conductivity," *J. Appl. Phys.*, 32, 1679-84, 1964.

[11] H. Lee, "Thermal Diffusivity in Layered and Dispersed Composites," PhD dissertation, 1975, Purdue University.

[12] John G. Bai, Zhiye (Zach) Zhang, etc. "DETERMINATION OF INTERFACIAL THERMAL RESISTIVITY BY FINITE ELEMENT MODELING OF THE FLASH MEASUREMENTS" *Itherm Conference 2004 Las Vegas.*

[13] D.A. Watt, "Theory of thermal diffusivity by pulse technique", Brit. J. Appl. Phys., vol. 17, pp. 231-240, 1966.

[14] J. Gembarovic and R.E. Taylor, use of Laplace transformation for data reduction in the flash method of measuring thermal diffusivity, Int. J. Termophys. vol. 14 no. 2, pp.297-311, 1993.

[15] K. Beadham and I.P. Dalrymple, "The measurement of thermal diffusivity by the flash method—an investigation into errors arising from the boundary conditions." Rev. Int. Hautes Temp. Refract. , pp. 178-283, 1970.

[16] J.A. McKay and J. T. Schriempf, "Corrections for nonuniform surface heating errors in flash method thermal diffusivity measurement, J. Pll. Phys. vol. 47, no. 4, pp. 1668-71, 1976.

[17] D.P.H. Hasselman and K.Y. Donaldson, "Effects of Detector Nonlinearity and Specimen Size on the Apparent Thermal Diffusivity of NIST 8425 Graphite", International J. of Termophysics, vol. 11, no. 3, pp. 573-85, 1990.

[18] S. Haque, "Processing and Characterization of Device Solder Interconnection and Module Attachment for Power Electronics Modules," PhD dissertation, 1999,Virginia Tech.