NEW WAY FOR THERMAL TRANSIENT TESTING

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ABSTRACT

This paper introduces a new concept of thermal transient measurement of IC packages, without a tester. The thermal transient test kit described here consists of a test chip, a dedicated software running on a PC and a special cable connecting the PC to the IC package which encapsulates the test chip. The functionality of a thermal transient test equipment is realized by the test chip itself and the measuring software. The software performs both the control of the measurement and the evaluation of the results. The final output of the evaluation software is a compact model network and the structure function, describing the properties of the heat conduction path realized by the IC package under test. The use of the test kit and the capabilities of its evaluation software are demonstrated by a few examples.

NOMENCLATURE

f	Frequency
T	Temperature in ^{o}C
γ	Sensor sensitivity
$a(t)$	Transient step-function response
z	Logarithmic time in Eqs. (2), (3)
$R(z)$	Time-constant spectrum, Eq. (2)
$w(z)$	Weight function in Eq. (3)
ρ_n	Cumulative thermal resistance
K_n	n-th value of the cumulative structure function
R	Thermal resistance
C	Thermal capacitance
k	The differential structure function

I. INTRODUCTION

The usual way to measure the thermal transient properties of packages is the recording of the package thermal transients: the thermal response to a step-function excitation.

There exist dedicated measuring equipment to carry out the recording of the thermal responses. These equipment consist of controlled voltage and current sources, sensing amplifiers, A/D converters, computer interfaces etc. The block diagram of such a tester is presented in Figure 1. The evaluation of the recorded responses is a question that many researchers have been dealing with for the last two decades – see e.g. [1], [2], [3], [4].

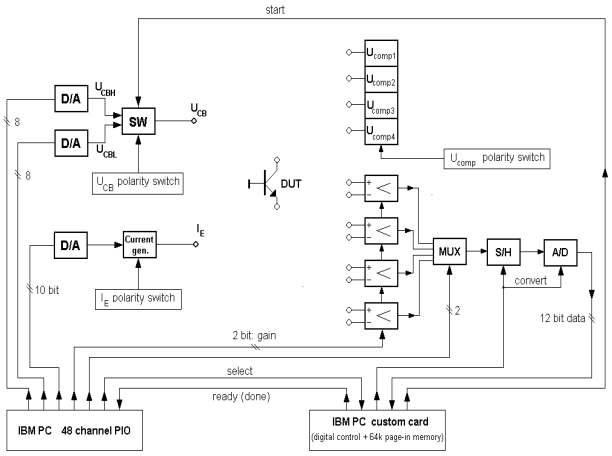

Figure 1 *Block diagram of a four-channel thermal transient tester [8]. The sensor & actuator chip that should be inserted into the package is a BJT.*

A complex measuring equipment, for the thermal transient experiments (such as shown in Figure 1) is expensive and clumsy. The purpose of this paper is to present an alternative solution for the method of thermal transient testing, much easier, cheaper and more flexible.

II. THE NEW CONCEPT

The investigation of the thermal transient properties of a package requires a certain amount of preparation. Some kind of thermal test chip is needed that has to be encapsulated into the package being measured. This test chip has to be provided with a temperature sensor and with a controllable dissipator element.

It is obvious that extremely simple test chip structures can meet these requirements. A pn junction diode as sensor and a resistance as dissipator are basically enough to carry out the thermal transient recording and this is the usual way of executing thermal transient testing today. But we believe that there is no reason to restrict ourselves to such simple test chips.

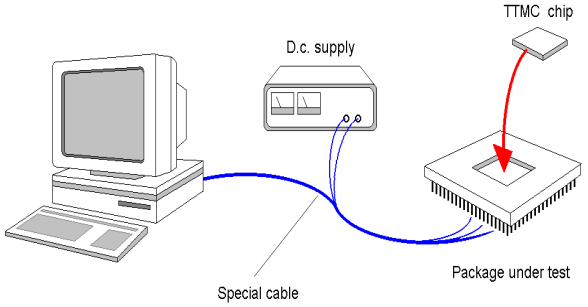

Figure 2 *Measuring arrangement realized without a thermal transient tester equipment*

The size of the test chip is determined by the package being investigated. In order to measure a package having a chip cavity of e.g. 10×10 mm we have to use a test chip that has similar size. This huge amount of silicon area allows us today to realize many blocks of the measuring circuitry on the test chip itself, forming earlier the part of the measuring equipment.

Our concept is extremely radical. We propose to eliminate *completely* the measuring equipment, by distributing all its functionality between two new dedicated supporting elements:

(i) an excess circuitry built into the thermal test chip, forming one part of the measuring hardware, and

(ii) a control software that runs on a PC and substitutes the other part of the measuring circuitry.

This way, practically all the expenses of the transient measuring equipment can be saved. The interface to the PC can be realized using the standard serial or parallel ports – no special card is needed. Only a small part of the measuring hardware cannot be realized neither on the test chip nor by software, namely the crystal oscillator needed for timing purposes. This part can be incorporated into an "intelligent measuring cable" connecting the chip to the PC. Obviously the power to heat the package must be provided by an external supply unit. The measuring arrangement is presented in Figure 2.

III. REALIZATION OF THE CONCEPT

A. *The design of the Thermal Transient Measurement Chip (TTMC)*

The first question was to find *the appropriate temperature sensor*. The conventional pn diode temperature sensor provides analogue output signal. This is a disadvantage, since in order to record temperature transients by a computer we need digital data. One solution is to use A/D converter circuitry realized on the chip. In our practice we follow another way. We use a digital (frequency) output CMOS temperature sensor that has been developed in our laboratory, and is very suitable to be built into CMOS designs to measure chip temperatures [5]. This sensor provides a square wave as output signal whose frequency depends on the temperature. This temperature dependency can be approximated as

$$f_{out} = f_{20Cels} \exp(\gamma\,(T_{Cels} - 20^{o}C)) \qquad (1)$$

where γ is the sensitivity, f_{20Cels} is the nominal frequency related to T=20°C. In the present realization of the sensor the sensitivity is γ= –0.79 %/°C, the f_{20Cels} frequency is about 1 MHz. The characteristic of Eq.(1) is valid between –40°C and 110°C with an accuracy of ±0.6°C [5].

The second problem is the *realization of the controllable dissipating element*. In our opinion the use of dissipating resistors is not practical since the on/off switching of these elements can not be realized by using logic signals directly: some further switching device is needed. From this point of view using heater MOS transistors is a better solution enabling direct logical control on their gates. A practical problem arises if the switching-on transient is measured, since the parameters of a dissipating transistor change with the temperature, resulting in a decrease of its current as the chip temperature increases due to the dissipation. It means, that providing a constant dissipation step is impossible. To overcome this problem, we measure the switching-off transient. From a given dissipation level we switch to a constant zero dissipation which is easy to assure. In this way, after a long heating up, when the chip temperature becomes stable, we switch off the dissipating transistors and we record the cooling-down response, instead of the heating-up transient.

The third problem is the *interfacing of the thermal measurement chip* to the computer. In the case of the realized chip we have chosen a standard solution: the boundary-scan (BS) circuitry, defined to enable standardized electrical testing of ICs and PC boards [6]. Figure 3 shows the microphotograph of the realized test chip.

Three excess BS instructions were used in the actual realization of the thermal test chip:

- **U7** Provides start signal for the sensor, resets the counter.
- **U8** Selects the temperature register as test data register into the BS path.
- **U9** Activates the dissipator transistor. (The way to deactivate the dissipator is to force the BS circuitry into the **Test-Logic-Reset** state.)

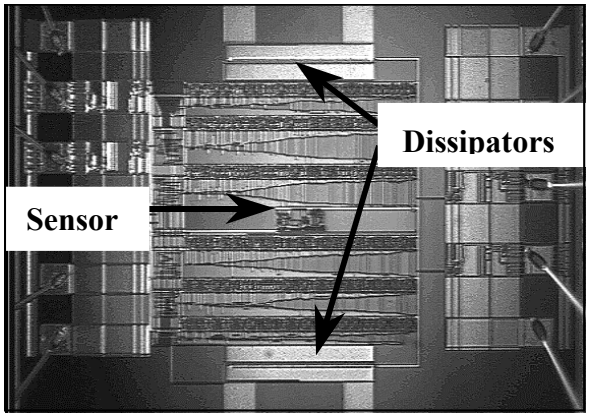

Figure 3 *The microphotograph of the test chip*

B. *The design of the software*

The first segment of this software serves for controlling the test chip. In order to make the things as simple as possible we use the parallel (printer) port of the PC to drive the test chip's inputs and to receive its output signal. The timing of the control is provided by a crystal oscillator that is part of the "intelligent measuring cable". This software realizes BS control sequences in order to switch-on and off the dissipators, to enable the sensor, to count the sensor frequency and to shift-out the measured data. According to the character of the thermal transient response, a quasi-logarithmic control of the sampling rate is desirable. This requirement can be easily fulfilled by the appropriate software control of the BS signals. The measured responses are finally stored in data files waiting for the evaluation.

The second segment of the software evaluates the measured responses. The method used for this evaluation is an adaptation of the method of Gardner [7], published recently in a number of journals and conference proceedings, e.g. [8], [9]. The principle of this evaluation method is described by the equation

$$\frac{da}{dz} = R(z) \otimes w(z) \qquad (2)$$

where $a(t)$ is the step-function response, $z = \log t$, $\otimes$ is the symbol of the convolution and

$$w(z) = \exp(z - \exp(z)) \qquad (3)$$

Applying the inverse operation of the convolution called *deconvolution,* Eq.(2) allows us to determine the $R(z)$ function. This function gives the distribution of the different time constants in the response.

Knowing this function it is already an easy task to construct thermal model for the package or to draw the *structure function* [2] which is the map of the heat flow path, reflecting sensitively the properties of the heat conduction path, e.g. any irregularities or defects of the heat removing.

The program provides a friendly user interface with different utilities for the quantitative evaluation, model generation, comparison between measurements etc.

IV. EXPERIMENTAL RESULTS

A measured thermal transient function is shown in Figure 4. This function was obtained by using a thermal transient measurement chip controlled by a PC through the printer port. *No measuring equipment* was needed to measure this function (except for a d.c. power supply unit).

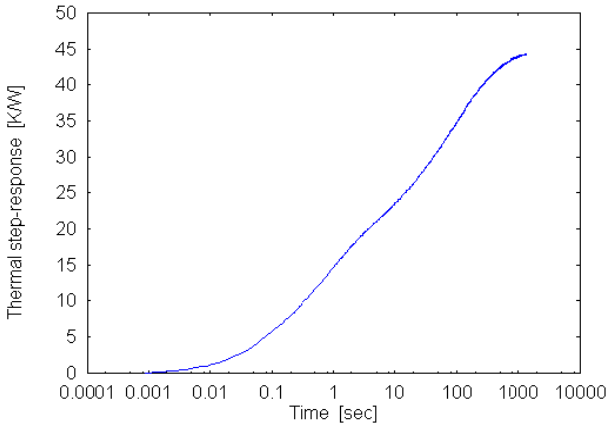

Figure 4 *Thermal transient response of a ceramic DIL package – recorded without a transient tester.*

The time resolution is obviously limited by the finite window of the frequency counting. When shorter time window is used the accuracy of the measurement degrades. The 1-2 ms (and perhaps variable) window gives however a good trade-off. The measured function shown in Figure 4 starts in the ms range and the SNR ratio of the temperature function is about 500.

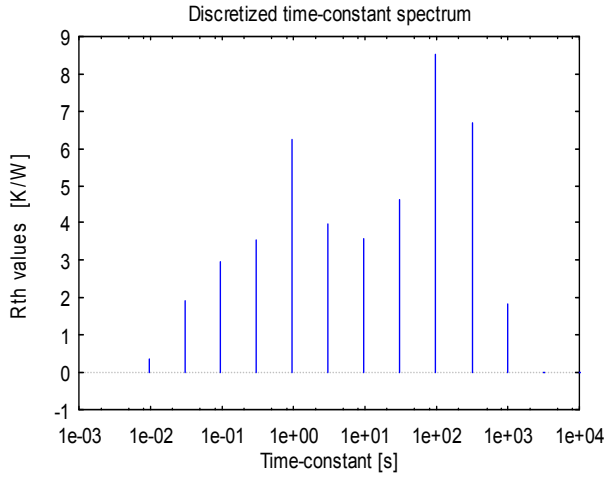

Figure 5 *Discretized thermal time-constant spectrum of the package, obtained from the response of Figure 4.*

In order to evaluate the thermal response a modified version of the THERMODEL program [10] has been applied. This program uses the evaluation method described in the previous paragraph. At first the time-constant spectrum of the package is extracted from the measured response. Such a spectrum is plotted in Figure 5 in discretized form (two time-constants per decade).

These data offer a direct way to build the dynamic thermal model of the package. A possible model network is the Cauer-ladder, see Figure 6. The ladder's thermal resistance and capacitance values are derived from the spectrum of Figure 5.

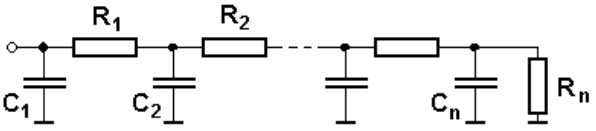

Figure 6 *Cauer-ladder modeling the thermal behavior of the package*

In order to verify the generated model the response of this model has been compared to the measured response. The two functions are plotted in Figure 7. The agreement between them is fairly good proving the accuracy of the model.

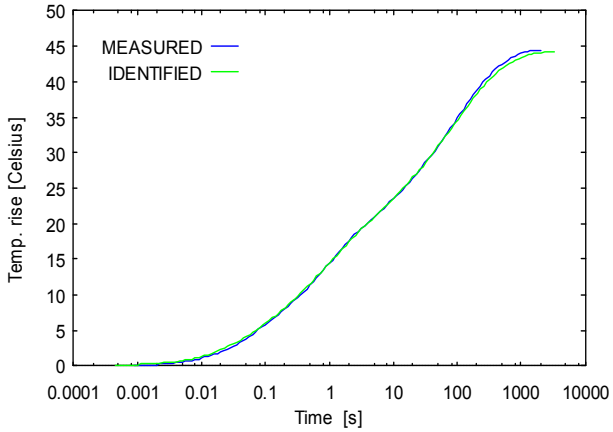

Figure 7 *Measured response and the response of the model network*

V. THE STRUCTURE FUNCTION AND ITS USE

The evaluation program is suitable also to generate the map of the heat-flow path between the chip and the ambience. Such a heat-flow map derived from the thermal response of Figure 4 is shown in Figure 8. This is the *cumulative structure function*, where the *x*-axis is the cumulative thermal resistance – starting from the chip, the *y*-axis is the cumulative heat capacitance.

The structure function is theoretically derived from the one-dimensional heat-flow equation, for details see [2], [12]. (One-dimensional here means *essentially one dimensional*, including cylindrical and spherical propagation, too.) In practice, it can be easily constructed from the Cauer-type model network shown in Figure 6. The thermal resistance between the *n*-th element of the model network and the heat source is

$$\rho_n = \sum_{i=1}^{n} R_i \qquad (4)$$

and the cumulative thermal capacitance is

$$K_n = \sum_{i=1}^{n} C_i \qquad (5)$$

where R_i and C_i denote the element values of the *i*-th stage of the Cauer-type model network. It can be proved (see e.g. [12]), that the derivative of K_n, the differential structure function

$$k = \frac{dK_n}{d\rho_n} \qquad (6)$$

is proportional to the square of the cross-sectional area of the conducting path.

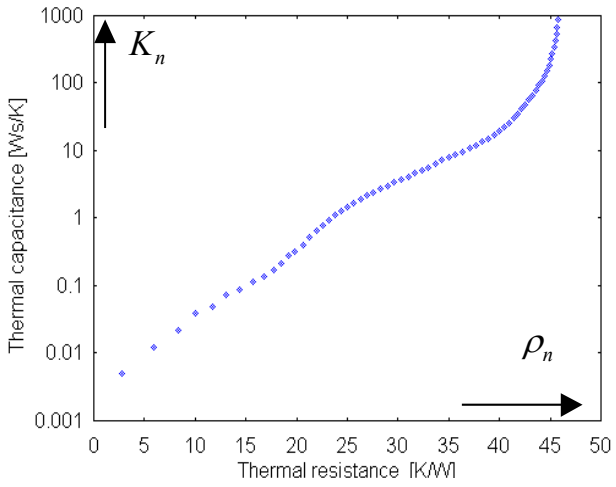

Figure 8 *Cumulative structure function of the heat-flow path. The left-hand side corresponds to the chip, the right-hand side to the ambience.*

The $k(\rho)$ differential structure function has some interesting features. For example, its integral is characteristic for the heat capacitance of a given section of the heat conduction path. More precisely, the total heat capacitance between two points of the structure characterized by parameters ρ_1 and ρ_2 is

$$C_{12} = \int_{\rho_1}^{\rho_2} k(\rho)d\rho \,. \qquad (7)$$

The physical distance between points of the structure characterized by parameters ρ_1 and ρ_2 is

$$x_{12} = \int_{\rho_1}^{\rho_2} \sqrt{\frac{\lambda}{\chi}}.k(\rho)d\rho \,, \qquad (8)$$

where λ and χ denote the thermal conductivity and the specific heat per unit volume of the material. (For further features and for the analytical form of the structure function in special cases refer to e.g. [12].) Values of k for different materials are given in Table 1.

Material	$\boldsymbol{k}$ [W^2 sec / K^2]
Silicon	$2.58 \cdot 10^8 \cdot A^2$
Iron	$2.65 \cdot 10^8 \cdot A^2$
Kovar	$0.70 \cdot 10^8 \cdot A^2$
Al_2O_3	$0.95 \cdot 10^8 \cdot A^2$

Table 1 k *values for different materials.* A *denotes the cross-sectional area.*

As it can be seen in Figure 8, the structure function tends to infinity, corresponding to the fact, that the "universe" as a general thermal environment has an infinite thermal capacitance. The distance between the origin and the location of this singularity of the structure function is exactly the thermal resistance between the heat source (in our case the test chip) and the ambience (which is 45 K/W in Figure 8).

The features characterized by relations (7) and (8) suggest, that the structure function is a good tool to identify geometrical dimensions of the heat conduction path if the material is known. The structure function can also be used to guess the type of the material of the heat conduction path in the knowledge of its geometrical dimensions, but in any case, the total chip-to-ambience thermal resistance of the structure can be identified with its help.

VI. CASE STUDIES

The first test chip encapsulated into a ceramic DIL package was used in various case studies. In one of our experiments we investigated the effect of an IC socket.

We had two setups, in which the only difference was, that the test chip was soldered directly into the test board or was plugged into an IC socket soldered into a similar PCB having the same geometrical and thermal properties. The final results obtained by our thermal transient test kit are shown by the structure functions plotted in Figure 9. The increased thermal resistance towards the ambience introduced by the socket is clearly visible on the plots. This value is about ΔR_{th} = 25 K/W (see the difference of the singularities of the curves).

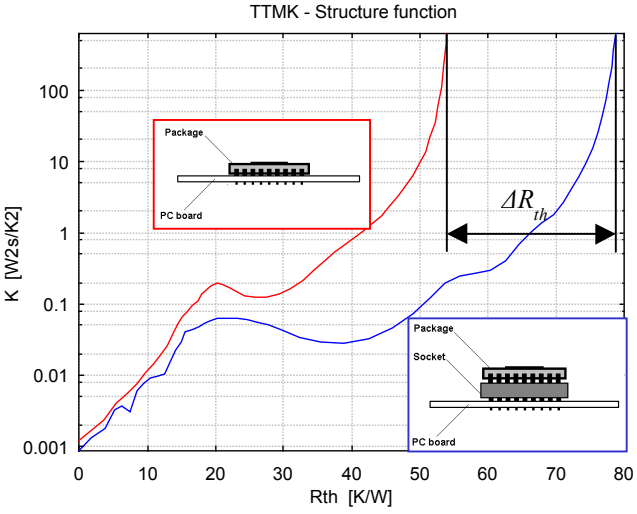

Figure 9 *Effect of a chip socket, demonstrated by the differential structure function.*

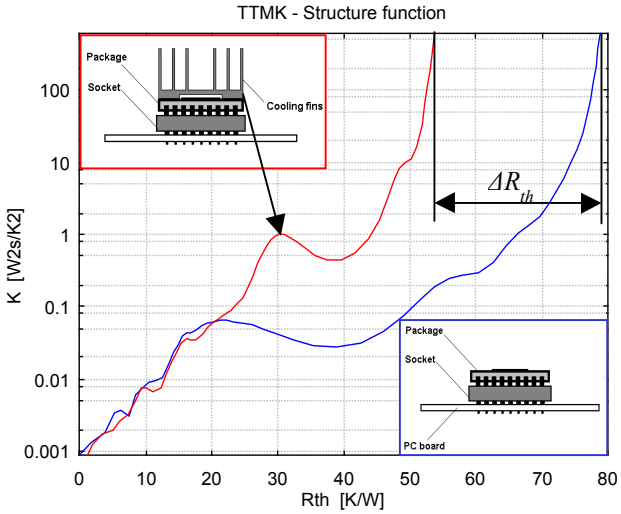

Figure 10 *Effect of a cooling mount, demonstrated by the differential structure function.*

In the second experiment the test chip was plugged into a socket and in one of the measurements a cooling mount was attached to the top of the IC package. The obtained structure functions are plotted in the same diagram in Figur1 10. This clearly shows that the cooling mount introduces an excess thermal capacitance (the corresponding "bump" in the structure function is marked by an arrow) as well as it reduces the thermal resistance by a great extent, compensating for the excess thermal resistance introduced by the IC socket.

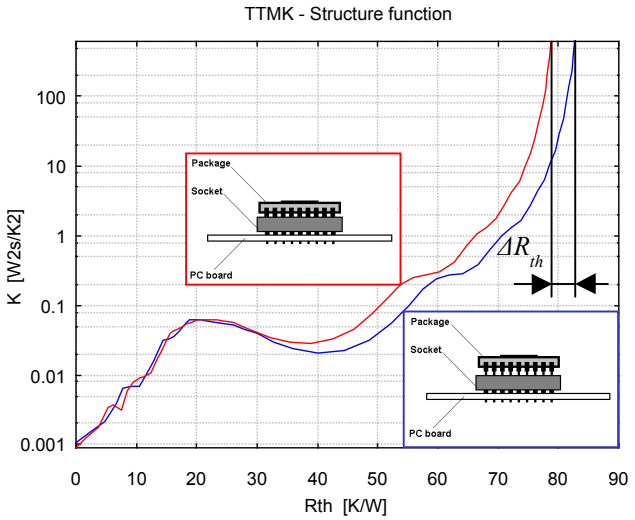

Figure 11 *Effect of the pin length*

A third experiment was performed in order to demonstrate the sensitivity of our test method. The same setup was used: the test chip plugged into an IC socket that was soldered into a printed circuit board. The difference between the two measurements shown in Figure 11 was, that in one case the test IC was fully plugged into the socket, while during the other measurement it was only slightly plugged in: to realize the electrical connections only. In this second case the heat removing path was extended by the extra pin-length that remained outside the socket. This excess heat resistance can be identified as the difference between the singularities of the two curves, which is about ΔR_{th} =5 K/W, corresponding to 1.5 mm excess pin length of the IC.

VII. DEVELOPMENTS IN PROGRESS

Besides the present version, we intend to realize some more sophisticated designs of the thermal transient measuring chip. The main goals of this development work are as follows:

- to make the sampling rate – accuracy trade-off less critical, either by increasing the sensor output frequency or by using more sophisticated frequency measuring method than the simple counting. The 10-11 bit resolution and 100-200 μs sampling rate are our present goals.
- The digital control of the amount of dissipation would be desirable.
- More uniform dissipation on the chip might be desirable
- The possibility of tiling of a larger surface area with smaller chips may be desirable

The evaluating software might be improved as well. The most important addition could be the support of the dynamic thermal model generation for the case of multiport package models [11], but this requires some more basic research on the subject.

VIII. CONCLUSIONS

The thermal transient measurement of the IC chips and packages can be carried out without using expensive dedicated tester. An appropriate toolkit is suitable to make these measurements, containing the following elements:

- Naked thermal transient measurement chips (TTMC-s) that have to be encapsulated into the investigated package. Whereas the packages have chip cavities of different sizes, a set of chips with gradually increasing size is needed. The dissipation of these

chips is controlled by digital signals and their built-in temperature sensor is read by using digital signal path – both of them are done by a PC program.

- A special cable that connects the thermal measurement chip to one (serial or parallel) port of a PC. This cable incorporates a minor circuit block: a crystal oscillator.
- A PC software, suitable to control the functions of the thermal test chip, to record the thermal transient functions and to evaluate the results.

Further hardware needs for carrying out the measurement are: an IBM compatible PC and an ordinary d.c. power supply – these units are usually available in an electronic laboratory.

The software is capable to determine the structure function and the thermal transient model of the package. Besides these, the d.c. thermal resistance of the package can be obtained as well. With a few examples it has been demonstrated, that the structure functions obtained by our thermal transient measurement kit are helpful tools to identify details of thermal properties of IC mounting on a PCB. These structure functions may help packaging engineers to design better IC encapsulations and may also help PCB designers to use mounting schemes with good thermal properties.

ACKNOWLEDGMENTS

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