Design of a multi-functional intelligent thermal test die

Zs. Benedek, G. Farkas, L. Pohl, A. Poppe, M. Rencz, V. Székely, K. Torki*, S. Mir*,

Budapest University of Technology & Economics (former TUB),
Department of Electron Devices, Budapest XI, Goldmann Gy. tér 3, H-1111 Hungary,
e-mail: rencz | benedek @eet.bme.hu

*TIMA Laboratory, 46, Avenue Félix Viallet, 38031 GRENOBLE Cedex FRANCE,
e-mail: <Kholdoun.Torki | Salvador.Mir | Bernard.Courtois>@imag.fr

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Abstract

Thermal characterization of IC packages and packaging technologies is becoming a key task in thermal engineering. To support this by measurements we developed a family of thermal test chips that allows a wide range of possible applications. Our chips are based on the same basic cell that is mainly covered by dissipating resistors and also contains a frequency output temperature sensor. These basic cells are organized into arrays of different size, controlled by the boundary scan circuitry. The arrays are designed such that larger arrays can also be built for tiling up larger package cavities. The first member of the family, TMC81 has been manufactured and the measurements show that all the goals aimed at the design have been achieved.

Objectives

Thermal test dies are among the major tools used in package thermal design qualification. They are usually simple chips, containing heaters and temperature sensors. The sensors measure the temperature on the chip surface as a result of the steady state powering, or the time dependence of the temperature increase or decrease in case of transient qualification. From these data the heat transfer properties of the package can be calculated and e.g. various cooling conditions can be evaluated easily.[1-4]

Thermal test dies are gaining increasing importance today in the thermal qualification of packages. This can be attributed to various components. On one hand to the fact that due to the increased power density in the packages the new packages are getting more and more sophisticated, needing more careful design and more complex test tools for the evaluation. On the other hand the parallel developing thermal transient measurement tools can measure simultaneously the temperature values at various locations, providing data for calculating the chip-inside thermal transfer parameters, consequently more sophisticated thermal test chips may be designed to support more complex measurements. [5] These new test chips could be today already computer controlled, enabling software controlled selection of the location of the active sensors within the package, and software controlled modification of the dissipation pattern of the chip. Such sophisticated thermal test chips - if they are measured with appropriate testers and evaluated by sophisticated software may deliver detailed data about the heat transfer properties within the chip itself and can be used also to qualify the die attach.

The objective of our work was to develop a *flexible and cost effective* solution for thermal characterization of IC packages and packaging technologies. We wanted to provide a set of actual test chips and IP designs of a scalable size starting from 2x2 mm^2 through 6x6 mm^2 up to a size of 24x24 mm^2. Besides producing the standard chip sizes demanded by the industry our major aim was providing the widest possible field of applications. We also had to conform the applying international standards (such as JEDEC JESD 51-4, prescribing among others the chip size, dissipation coverage, sensor diode positions, and IEEE 1149.1 specifying built in serial test circuitry for integrated chips, i.e. boundary scan standard).

General considerations for the design of the whole chip family are given in [6]. In the present document we focus on the design of two chips, TMC9 and TMC81 and on the measurements with the TMC81 thermal test chip, the first chip in the family realized by CMP.

1. Specifications

The general specifications we set forth before we started the design were as follows:

- Scalable chip size,
- Programmable dissipation patterns, including full dissipation coverage,
- Pattern of dissipators defined via boundary scan path, dissipation switched on and off by an asynchronous external signal,
- High dissipation level with homogenous distribution,
- High precision sensor elements with analogue and/or digital output,
- Boundary scan input and output as well as analogue output,
- Thermal measurement with the test chip without external tester equipment,
- High precision static measurement and high resolution transient measurement,
- Variable chip sizes and 85 % coverage with dissipating elements as recommended by the JEDEC standard,
- Cost-effective multi-project-wafer realization, using a standard, mainstream CMOS process,
- Core layout, pad arrangement and control structures allowing a physical tiling of larger package cavities using smaller test chips.

2. Structure of the test chips

As shown in the example of Figure 1 in RENVFUSIONFORMATour designs most of the chip area is covered by an array of identical basic cells (Figure 9b*SEQARABESEQARABE*). Each cell contains heater resistors and a digital output temperature sensor. As a further, facility sensor diodes are placed at the chip center, edges and corners as described in the JEDEC standard. These diodes are directly connected to analogue pads.

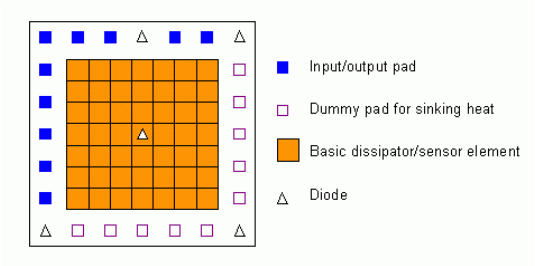


Figure 1 The overall design of the multi-functional thermal test chip

*SEQARABESEQARABE*The basic dissipation element is based on polysilicon resistors that consist of separate strips connected in series by metal (Figure 2). RENVFUSIONFORMATA large MOS transistor switches each dissipating resistor. RENVFUSIONFORMATSome design details are given in [6,14].

The size of a basic cell is 500x500 m ^{2}. Note, that even with an opening for the temperature sensors and the gaps between resistor strips the area coverage of the dissipators is above 87%, meeting the 85% coverage requirement of the JEDEC standard. We carried out thermal simulations by the SUNRED program [8] for checking the uniformity of the temperature distribution

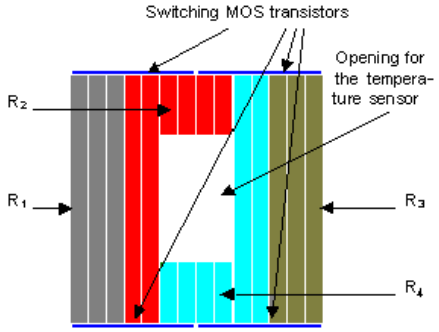


Figure 2 The dissipator structure SEQARABESEQARABE

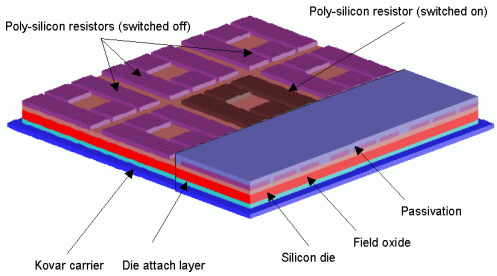


Fig.3. The build-up of the structure used to analyze the temperature field below a dissipator cell. (Figure not in scale)

SEQARABEWe assumed a 2x2 mm^2 structure that corresponds to the physical realization of TMC9 (Figure 3), but can also be used as a simulation model for larger chips [6].

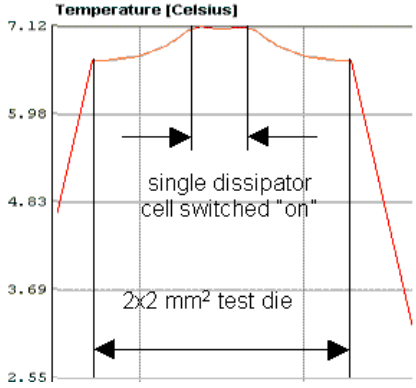


Figure 4 Temperature distribution on the silicon surface. Note the highly uniform temperature under the structure shown in Figure 2SEQARABE

Simulation results show that polysilicon resistors above the oxide layer provide a highly uniform temperature distribution on the silicon surface below a dissipator cell, even in the opening (Figure 4) SEQARABE

In each cell of the test array in the core area of the chip, a temperature sensor element is also placed which is the most recent version of our frequency output CMOS temperature sensor [9,14]. The operation of the sensors can be individually enabled and their square-wave output signal can be measured directly on analog outputs, or can be shifted out as a digital code word through the serial scan path.

Actual chip sizes and numbers of sensors and dissipators are given in Table 1. The realized TMC81 is of size 6x6 mm^2 and has 81 sensor/dissipator elements in its core.

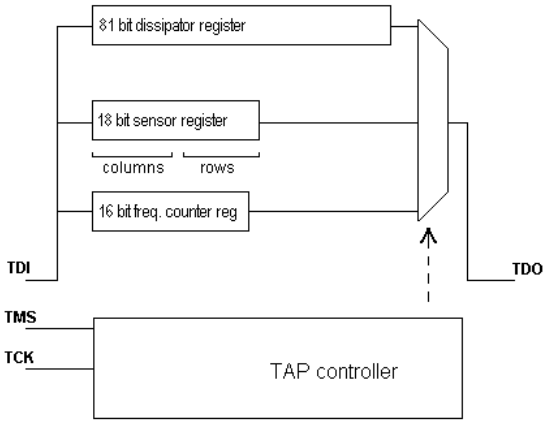


Figure 5 Draft of the boundary scan circuitry in the TMC81

In the TMC81 design the digital interface for programming dissipation patterns and accessing temperature data of the CMOS temperature sensors is provided by a boundary scan circuitry. As defined in the IEEE 1149.1 standard, this circuitry enables simple and efficient testing of all ICs on a printed board. These ICs have serial control and data registers that can be handled by altogether four signals: two input signals (TMS, TDI), an output signal (TDO) and a clock (TCK). Programs can carry out sophisticated functional measurements on ICs and printed boards through standard PC ports [5] using this interface.

In this design the boundary scan circuitry is composed of standard cells positioned outside the measurement area (as shown in Figure 9a). The required dissipation coverage is achieved even with this interface circuitry between the pad ring and the thermal core.

Figure 5 shows the draft of the boundary scan circuitry scheme. The Test Access Port (TAP) controller selects one of the three registers for controlling the measurement. Filling up the dissipator register defines the pattern of 9x9 dissipators switched on. The sensor register uses a row-column select scheme. The output of the selected sensor drives the counter register, captured values can be shifted out on TDO.

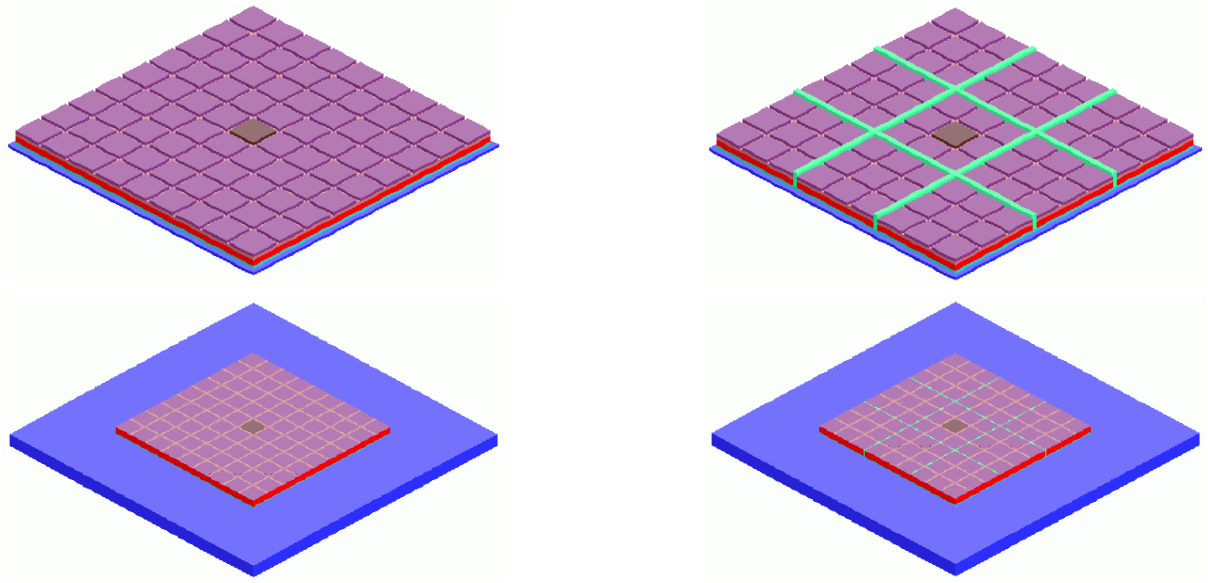
3. The scaling problem: tiling and composite design

There are two related approaches for producing larger covered areas in a package.

One concept is using small chips as elementary tiles for covering arbitrary oblongs in a cavity. This tiling method is rather efficient but raises several problems.

One of the problems is that in order to provide continuous signals chip-to-chip bonding is required.

Another possible problem is that using a patterned dissipation scheme a lateral heat-flow is expected as pointed out in [7,15] – chip tiles may have a rather large thermal resistance in lateral direction.

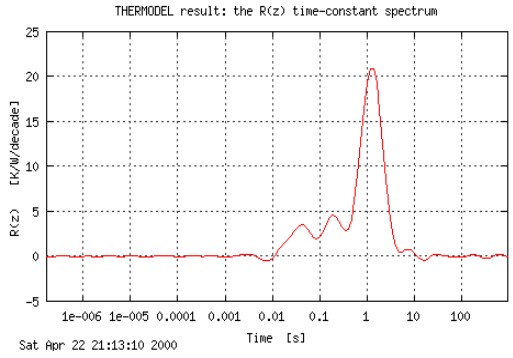


RENVFUSIONFORMAT*a)* *b)*

Figure SEQARABE6 The simulated structures drawn on a uniform grid and drawn with their physical dimensions: a) single 6x6mm^2 chip with 9x9 basic cells, b) chip cavity tightly tiled with 3x3 chips of an area of 2x2 mm^2, each having 3x3 basic cells

A preliminary thermal simulation study was carried out with the SUNRED program [8]. Our goal was to predict what are the measurements where we can we replace a “large” test chip by tiling the same cavity area with the appropriate number of small, 2x2 mm^2 dies. (SUNRED simulation models are shown in Figure 6RENVFUSIONFORMAT). Such a solution will have financial advantages over the large chips, since the small chips could be fabricated in larger volumes, decreasing the overall costs of the test die.

We found that in case of thermal transient measurements with power-step excitations applied to the whole active dissipating area no significant difference can be observed between the results obtained by the application of a large test die or by tiling the cavity with small dies.



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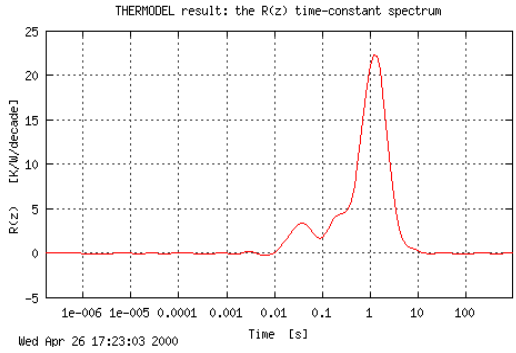

b)

Figure 7 Time constant spectra for excitation applied to the entire surface: a) single chip case, b) tiled case – the obtained spectra are essentially the same

Results of time-constant spectrum calculations obtained by the THERMODEL program [10] (shown in Figure 7*SEQARABESEQARABE*) support this statement.

TMC9, a 2x2mm^2 JEDEC compliant chip having a 3x3 sensor/dissipator matrix and a simple control logic is now in the foundry. These chips will be suitable for cost effective applications and for cavity tiling.*SEQARABESEQARABE*RENVFUSIONFORMAT

The other concept is using monolithic chip composites cut out from the wafer. In this case no internal bonding is required until the array size remains less than 2x2 chips.RENVFUSIONFORMAT Figure 8 illustrates a chip array that implements a composite design with four instances of the same TMC81.

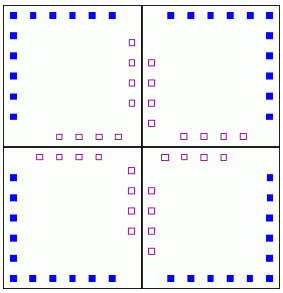

Figure 8 Composite designs containing four basic designs (with any size given in Table 1)

RENVFUSIONFORMATTable 1 summarizes the size of possible composite designs (assuming different chips as base, including TMC81) along with their current consumption and the available dissipation levels.

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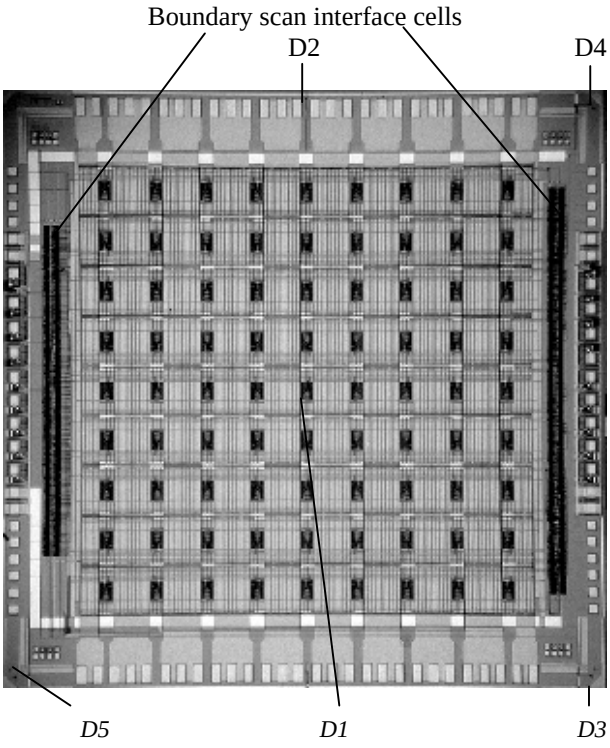
This table contains the measured values for the single TMC81 and the calculated values for planned chips and composites.

Table 1: Main parameters of composite designs with current/dissipation levels

Base chip	Composite design (**array**, area)	Dissipation (predicted)	Current	Dissipation (measured)	Current (measured)
6x6mm², ***9x9 cells***	**-** 6 x 6 mm²	6.4 W	1.3 A	6.6 W @ 5V 9.6 W @ 6V	1.32 A 1.60 A
	1x2 6 x 12 mm²	12.8 W	2.6 A		
	2x2 12 x 12 mm²	25.6 W	5.2 A		
9x9mm², ***15x15 cells***	**-** 9 x 9 mm²	18 W	3.6 A		
	1x2 9 x 18 mm²	32 W	7.2 A		
	2x2 18 x 18 mm²	64 W	14.4 A		
12x12mm², ***21x21 cells***	**-** 12 x 12 mm²	35.3 W	7 A		
	1x2 12 x 24 mm²	70.6 W	14 A		
	2x2 24 x 24 mm²	141.2 W	28 A		



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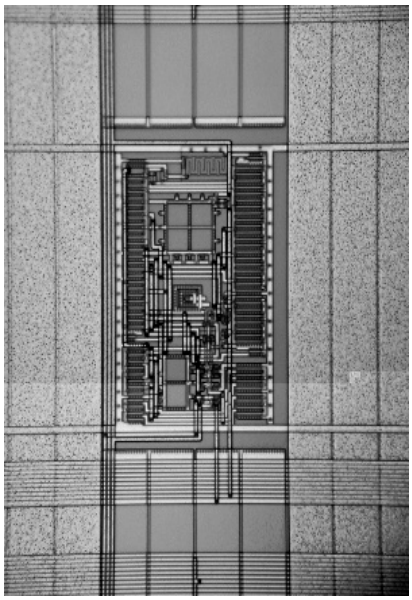


b)

Figure 9 SEQARABESEQARABEMicro-photographs of the manufactured chip: a) the 6x6 mm2 design, b) close-up view of a dissipator-sensor cell

4. Usage

The realized test chip structure allows the following measurements:

- **Measurement of steady-state temperature distribution** on the chip surface with *full dissipation coverage* or *patterned dissipation excitation* (pattern set via the boundary scan path):
  - Continuous parallel measurement using the sensor diodes.
  - Sampled measurement with serial shifting out at every matrix location using the CMOS sensors.

- **Conventional thermal transient testing** with a thermal transient test equipment (such as the ***T3Ster*** equipment [12]) using sensor diodes with *full dissipation coverage* or *patterned dissipation excitation:*
  - single temperature measurement on a diode
  - multi-port measurement

- **Thermal transient testing without a tester** ("tester on the chip" principle) such as realized with the TTMK Kit [11] using *full* or *patterned dissipation coverage*; measurement by a CMOS sensor at a single, program selected point (e.g. the middle) of the cell array, read-out via the boundary scan path.

5. Evaluation of the chip

The chip has been manufactured with a standard 0.8 micron CMOS technology of AMS[1].

Figure 9 shows pictures of the test chip fabricated. Figure 9a shows the whole chip area and Figure 9b is a part of the matrix element (cell) showing the CMOS sensor in the middle surrounded by polysilicon resistors.

A series of measurements have been carried out for evaluating the fabricated chips. Here we show some results corresponding to the measurement alternatives given in the previous section.

We started the measurements with an analysis on four chips from an MPW run.

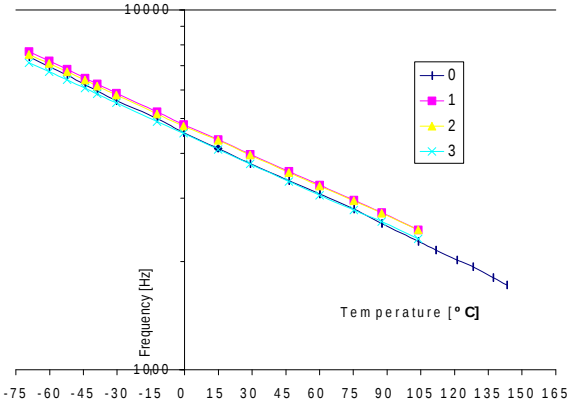
The sensor and dissipator characteristics were measured on chips encapsulated in ceramic PGA144 packages. The chips were plugged into a printed board with sockets and some additional selector circuitry.

The board was placed into a thermostat chamber. The measurement was made in the range from -75 to +140 centigrade, in a steady nitrogen flow. We measured steady-state frequencies, dissipator U-I characteristics and diode characteristics at all temperatures.

Theory shows that these sensors have approximately exponential characteristics [7,14]:

$$f = f_0 \exp(\gamma(T-T_0))$$

SEQARABEFigure 10 presents the measured frequency versus temperature curves on the middle sensor of the chips. We can observe the exponential character of the functions in lin-log coordinates, where we get straight lines, of course.



INCORPORERINCORPORER*Figure SEQARABESEQARABE10 Sensor characteristics of the TMC81, between -75 °C and +140 °C*

The f_0 and γ values were derived from the series of measurements and calibration files were produced for the chips. We found that f_0 values slightly differ even in one chip (at Chip1 standard deviation 2.1 % < =84 kHz> at 25 °C) but γ values are quite the same for all sensors (at Chip1 mean value $-6.6793*10^{-3}$ 1/ °C, standard deviation 0.616 % at 25 °C).

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[1] AMS Austria Mikro Systeme International AG, Austria

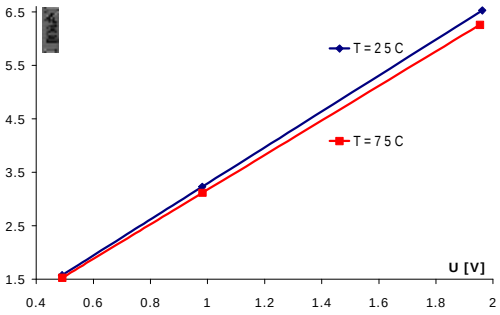

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Figure 11 Dissipator characteristics at 25 °C and 75 °C

The voltage-current characteristics of the dissipator elements can be seen in the Figure 11. The average resistance is about 300 , the saturation voltage of the MOS switches lies at 20 mV. The temperature dependence of the resistance is shown in Figure 12.

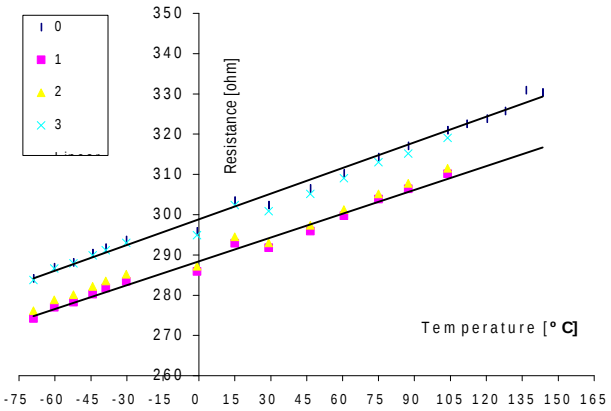

Figure 12 The temperature dependence of dissipator resistors

Figure 13 shows the measured characteristics of the diode sensors.

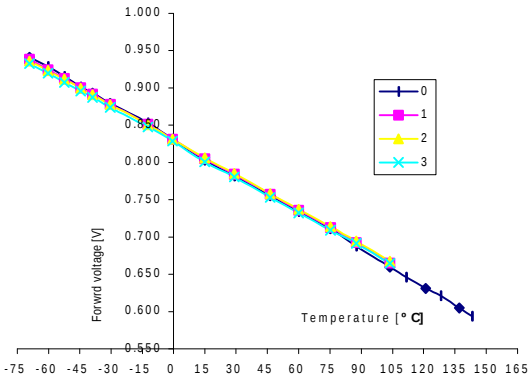

Figure 13 The characteristics of the diode sensors

Figure 10 and Figure 12 suggests that Chip0 and Chip3 are probably from the same wafer and so are Chip1 and Chip2.

Finishing the basic characterization above several measurements were carried out. Here we would like to present a steady state and a transient measurement on a TMC81 chips encapsulated in a PGA 144 package and placed in a standard 1 cubic foot still air chamber. Figure 14 shows the dissipator arrangement. Temperature was measured at all 81 CMOS sensors and at the three diodes indicated in the figure using a T3Ster equipment [12,16].

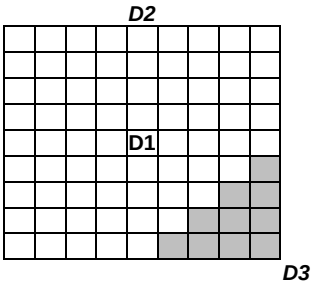

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Figure 14 Dissipator and sensor diode arrangement in the measurements

The measurement started with a 1000 sec period of temperature equalization. Then a power step of 0.68 W (4.5 V, 152 mA) was applied with the pattern presented and a 1100 sec heating curve was measured. The transient response can be displayed in different ways. Figure 15 shows a part of the transient measured on the diode type sensors by the T3Ster equipment [12,16].

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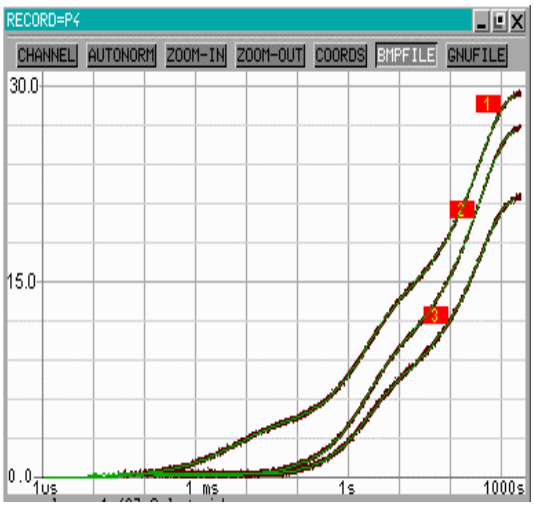

Figure 15 Transient response of the three diodes

Figure 16 shows the results of a transient measurement of three cells by frequency output sensors read through the boundary scan circuitry, with no tester equipment. The excitation was the pattern of Figure 14. Cells are indexed as {row, column}, i.e. 1,1 means the upper left corner.

In case of the T3Ster measurement the resolution is 1 µs and 12 bits at the analog diode sensors while 300 µs and 11-12 bits can be achieved with the measurements using the frequency output sensors.

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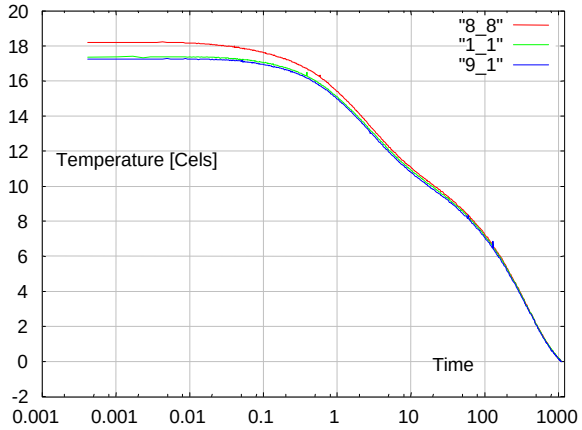

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Figure 16 Transient measurement on CMOS sensors at locations {8,8}, {1,1} and {9,1}

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In a different measurement type the software can make several readouts in a second of the whole temperature map of the chip. Such results are shown in Table 2 and Figure 17.

In this measurement we applied the dissipation pattern of Figure 14 again, now with a total power of 1W. In order to minimize small thermal fluctuations a reference frequency map was stored at the end of a 1000 second equalization period.

Table SEQARABE2 Differential temperature distribution on the chip

TEMPERATURE DIFFERENCE after 30 sec

				11.7				
11.28	**11.37**	**11.50**	**11.68**	**11.78**	**11.93**	**12.02**	**12.16**	**12.21**
11.39	**11.48**	**11.65**	**11.82**	**11.96**	**12.13**	**12.26**	**12.37**	**12.39**
11.66	**11.81**	**11.96**	**12.18**	**12.35**	**12.67**	**12.87**	**13.00**	**13.07**
11.76	**11.95**	**12.09**	**12.38**	**12.63**	**12.93**	**13.09**	**13.35**	**13.42**
12.02	**12.23**	**12.43**	**12.81**	***13.10***	**13.57**	**13.91**	**14.32**	**14.54**
12.11	**12.30**	**12.61**	**12.99**	**13.37**	**13.89**	**14.31**	**14.94**	**15.45**
12.27	**12.48**	**12.80**	**13.32**	**13.84**	**14.65**	**15.37**	**16.48**	**16.50**
12.34	**12.56**	**12.88**	**13.42**	**14.01**	**14.97**	**16.06**	**16.81**	**16.78**
12.36	**12.62**	**12.97**	**13.54**	**14.18**	**15.58**	**16.17**	**16.58**	**16.47**

13.7

Table 2 shows the temperature change on the chip measured and displayed by the control program 30 seconds after switching on the power. The table also shows the analog values measured on the diodes (in Italics).

Figure 17 also illustrates the display options of the control program – numeric measured data like in Table 2 can also be displayed as 2D or 3D temperature maps or temperature movies.

An evaluation program provides up-to-date characterization methods as the time constant spectrum and complex impedance loci of the packaged chip [12,15].

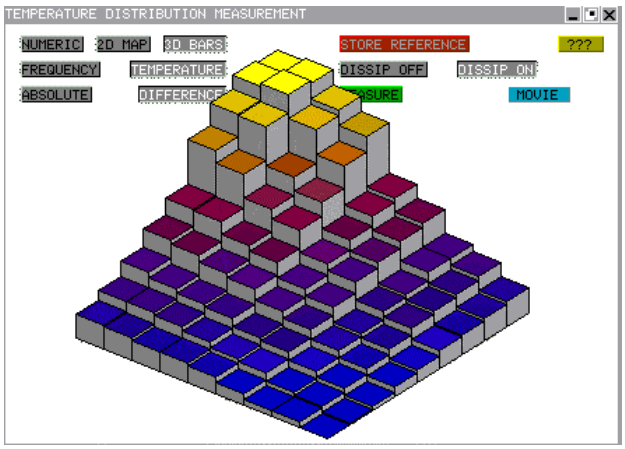

Figure 17 3D presentation of a measured temperature distribution in the control program

In Figure 18 we show the differential structure function derived from the transient curve of the dissipating point at row 8 column 8 (Fig 14) as an example.

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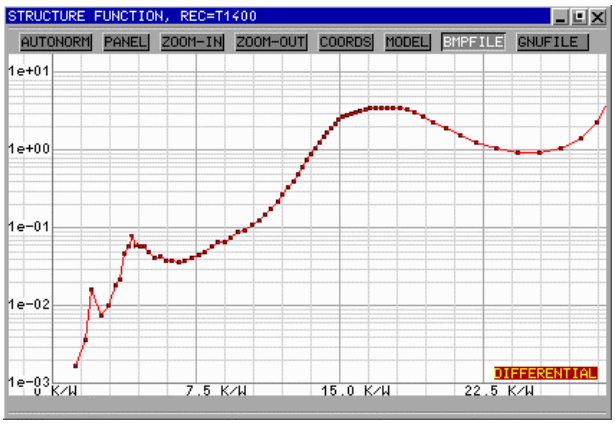

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Figure 18 Differential structure function of the packaged chip

This extremely useful function shows C_{th}/R_{th} as a function of the cumulated thermal resistance starting from the heat source and is roughly the cross-sectional area plot along the heat-flow path. For more reference see [12,16].

6. Conclusions

The presented new thermal test-chip design that provides scalability as well as a wide range of measurement options offers a new tool for package designers to qualify package designs. It has the potential for various other uses in the thermal design of microelectronics, e.g. the optimization and characterization of various cooling methods. There is a broad interest towards the test chip, even Intel [17] expressed their interest in it. MicReD[18] has plans to commercialize the design.

In the near future we plan to develop a family of test chips – partly in form of actual chips, partly in form of IP products to meet needs for large chip sizes. The first member of the IP product line has also been manufactured in order to allow the demonstration of the capabilities of the design. The measurements show that the chip fulfills or even over-performs the original aims.

7. Acknowledgments

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